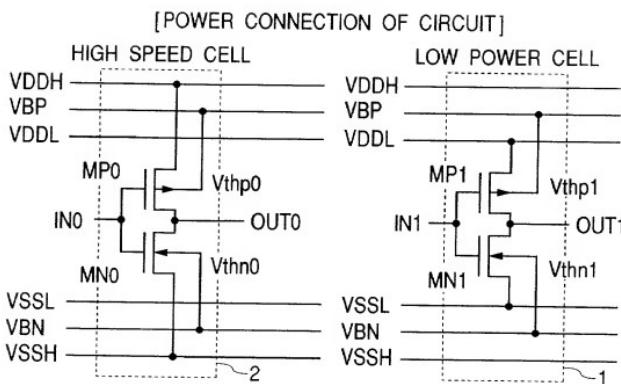
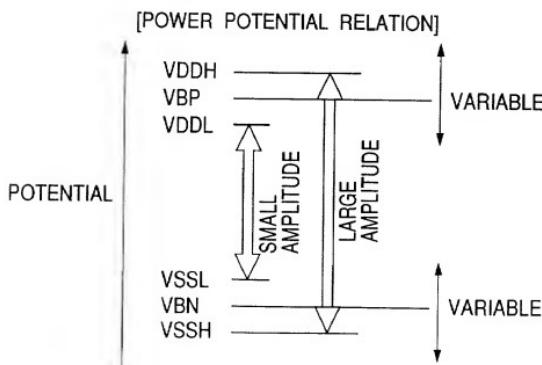
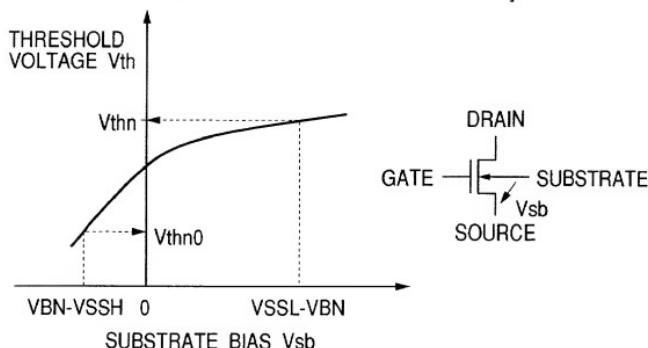


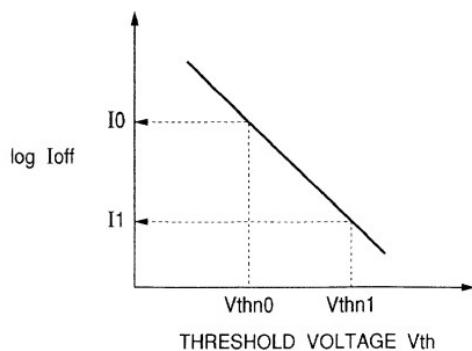
**FIG. 1****FIG. 2**

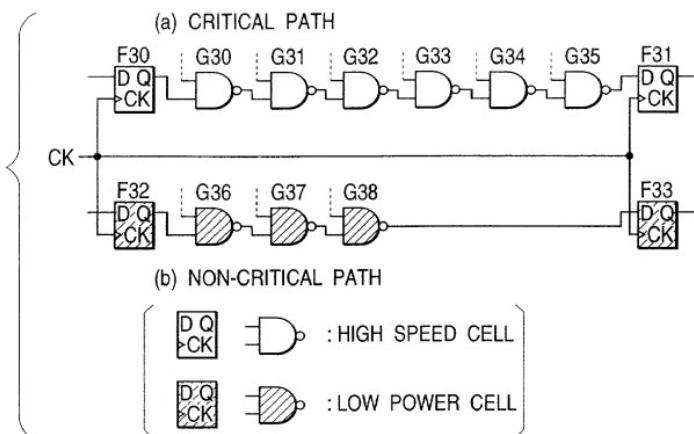
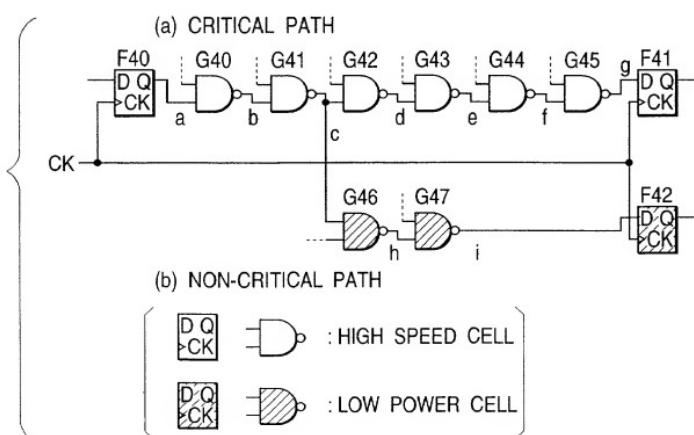
***FIG. 3***

[INCREASE IN THRESHOLD VOLTAGE BY APPLICATION OF SUBSTRATE BIAS]

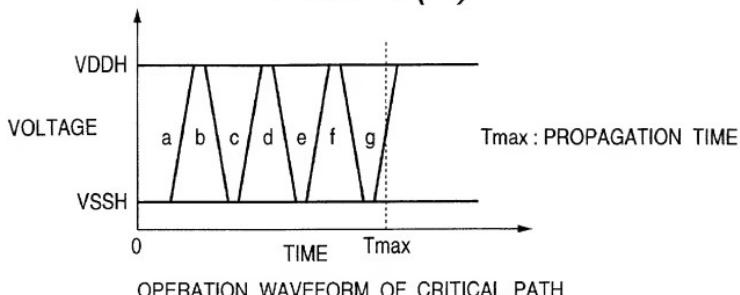
***FIG. 4***

[DECREASE IN LEAK CURRENT BY INCREASE IN THRESHOLD VOLTAGE]



**FIG. 5****FIG. 6**

*FIG. 7(A)*



*FIG. 7(B)*

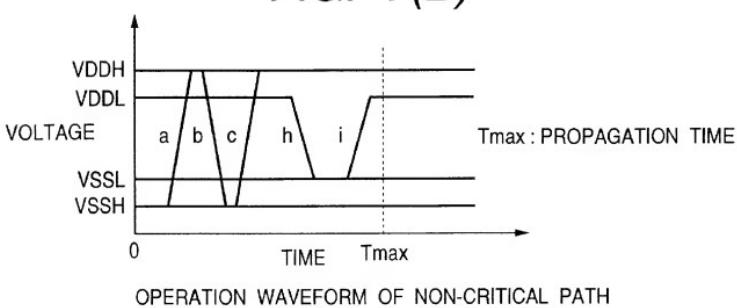
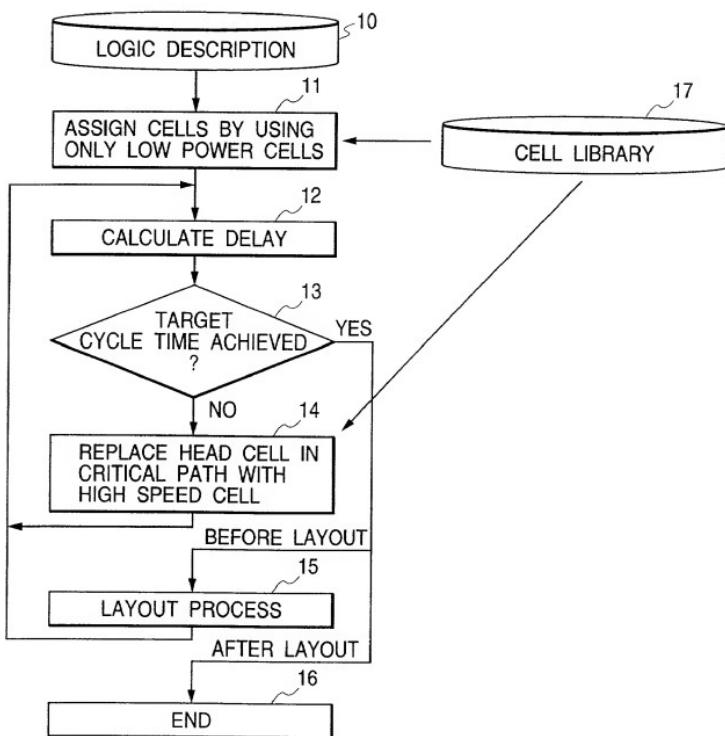


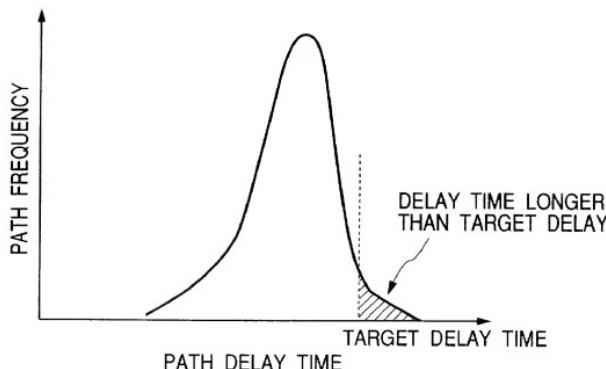
FIG. 8



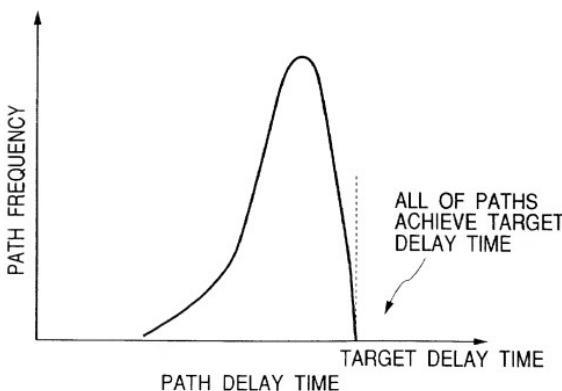
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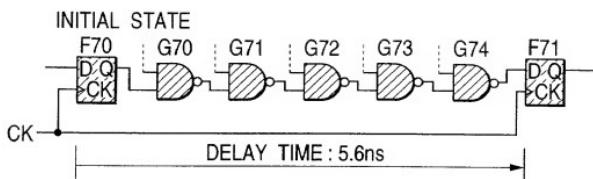
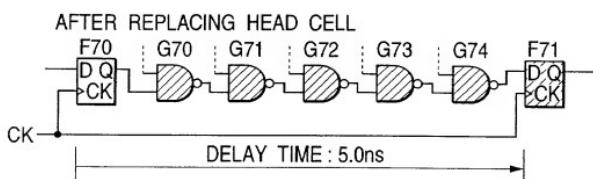
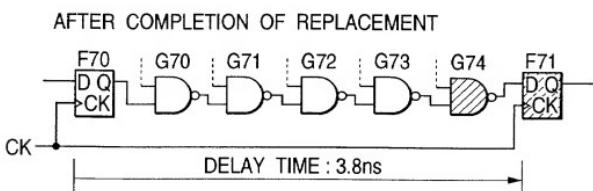
***FIG. 9(A)***

[CASE USING ONLY LOW POWER CELLS]

***FIG. 9(B)***

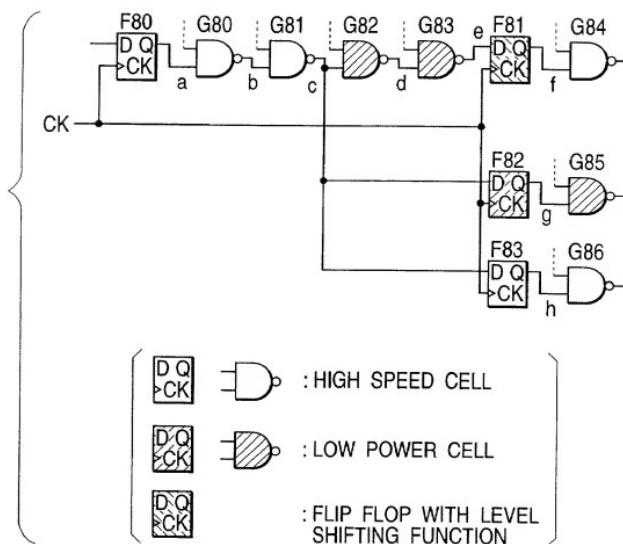
[CASE USING HIGH SPEED CELL FOR CRITICAL PATH]



**FIG. 10(A)****FIG. 10(B)****FIG. 10(C)**

 : HIGH SPEED CELL  
 : LOW POWER CELL

FIG. 11



**FIG. 12**

[FLIP FLOP WITH LEVEL SHIFTING FUNCTION]

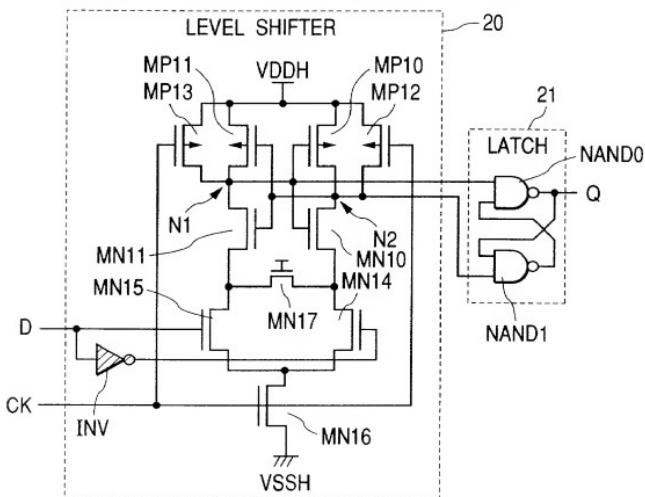
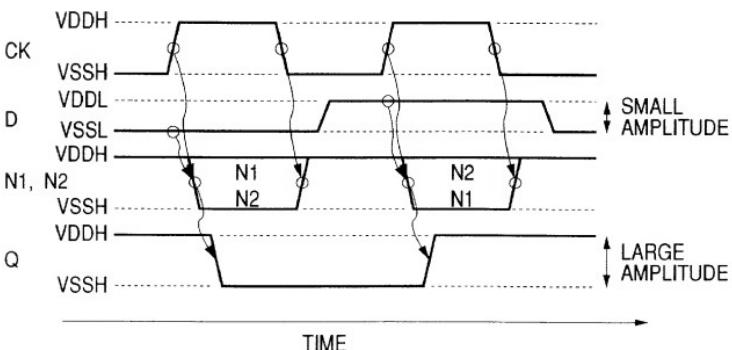
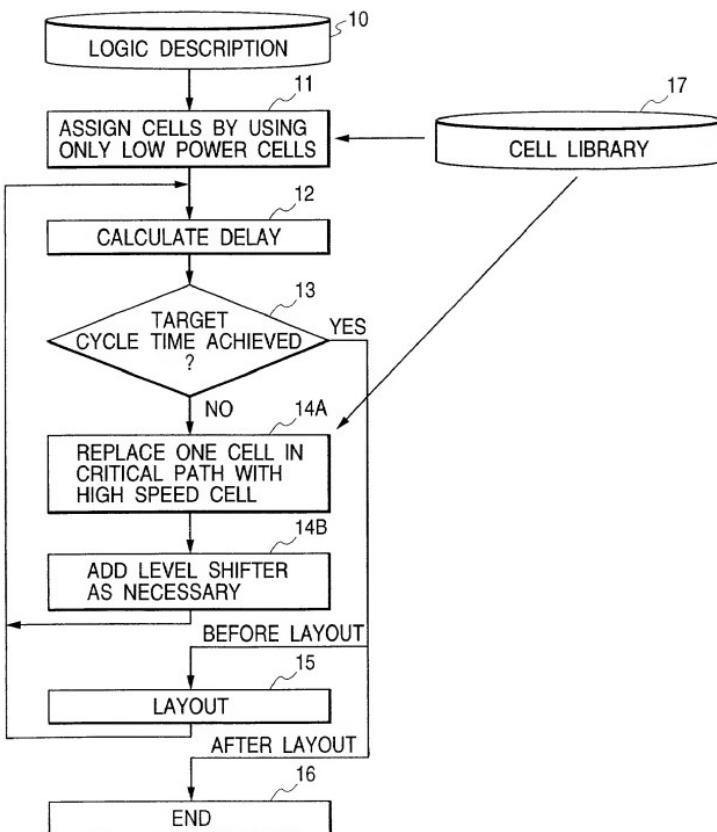
**FIG. 13**

FIG. 14



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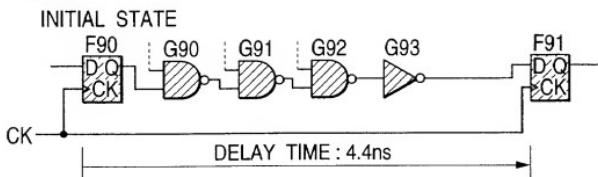
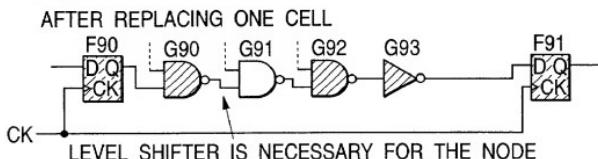
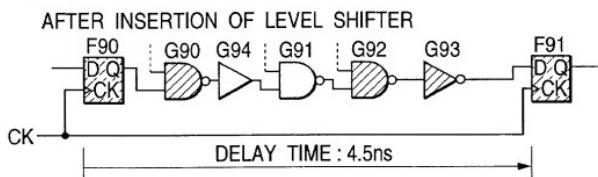
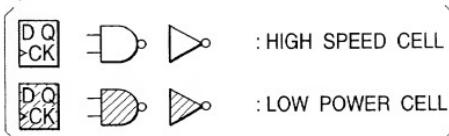
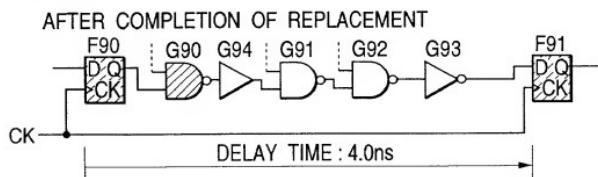
**FIG. 15(A)****FIG. 15(B)****FIG. 15(C)****FIG. 15(D)**

FIG. 16

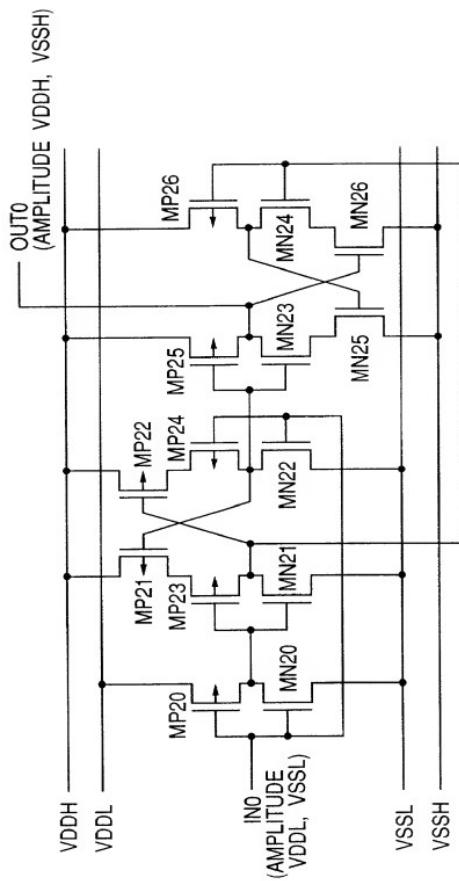


FIG. 17

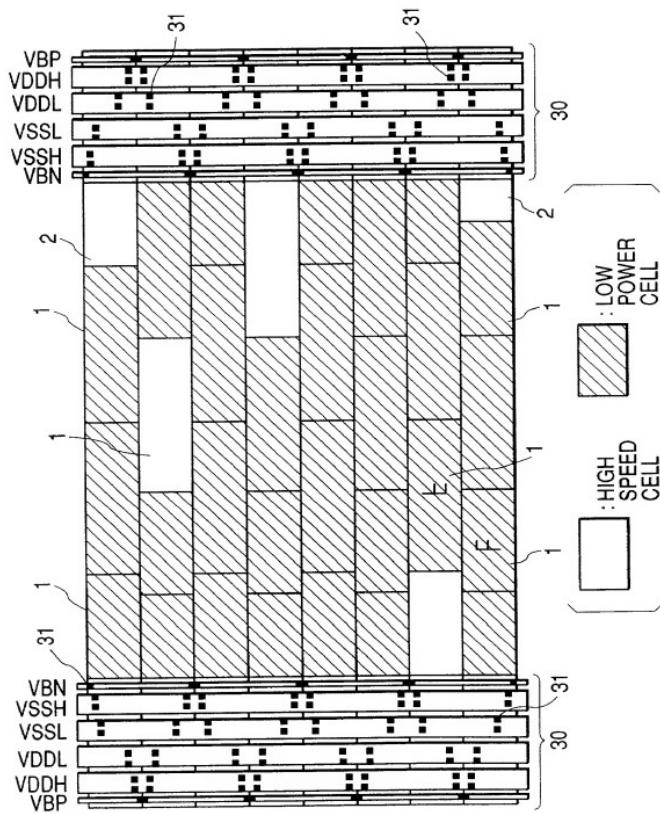


FIG. 18

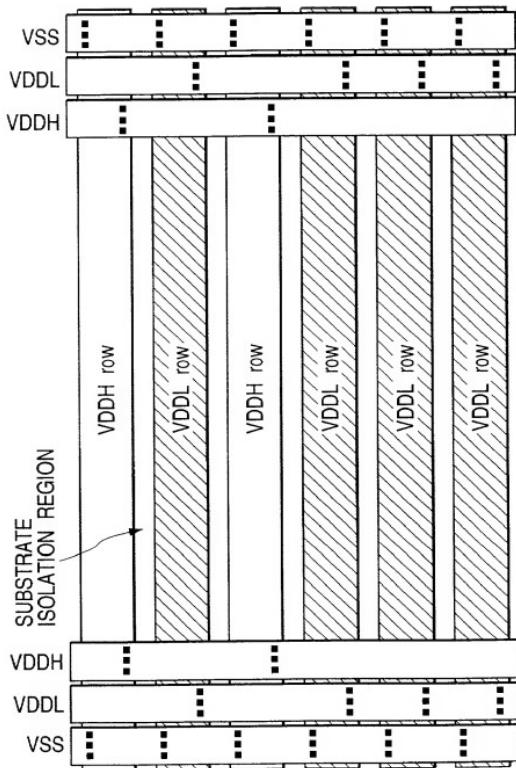


FIG. 19(A)

### [CONVENTIONAL CELL LAYOUT]

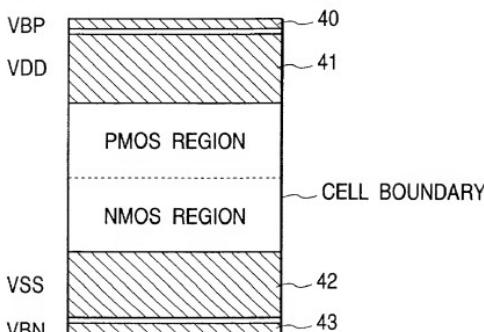


FIG. 19(B)

[CELL LAYOUT OF THE INVENTION]

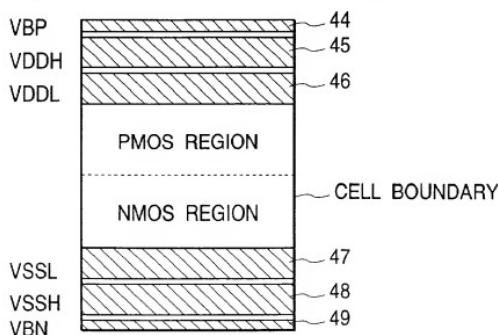


FIG. 20(A)

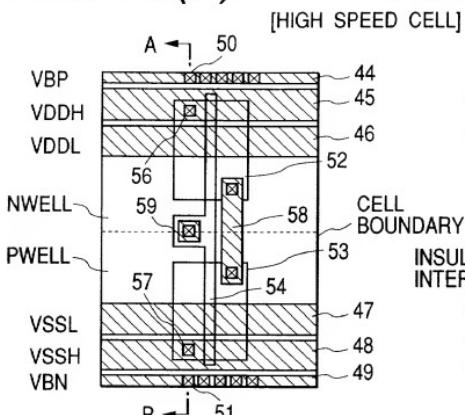


FIG. 20(B)

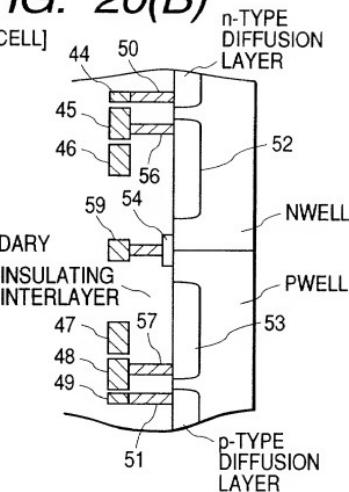


FIG. 21(A)

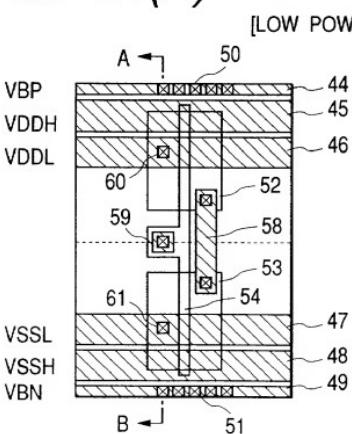
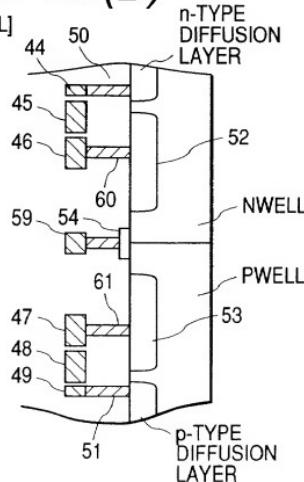


FIG. 21(B)



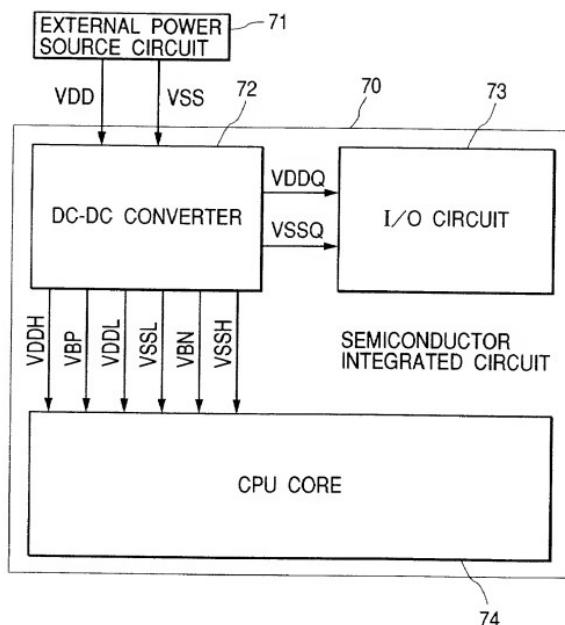
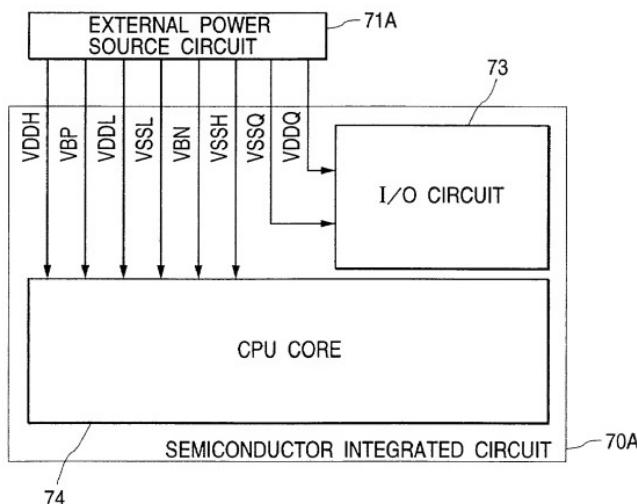
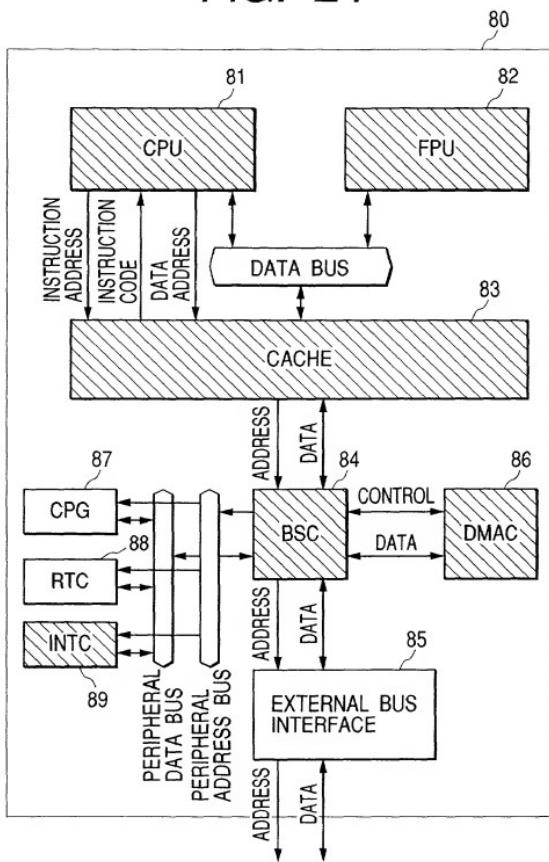
**FIG. 22**

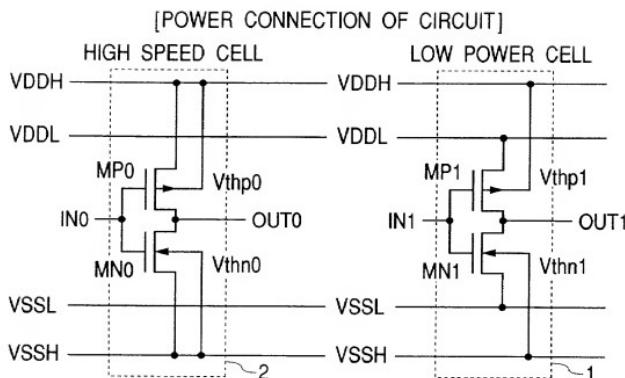
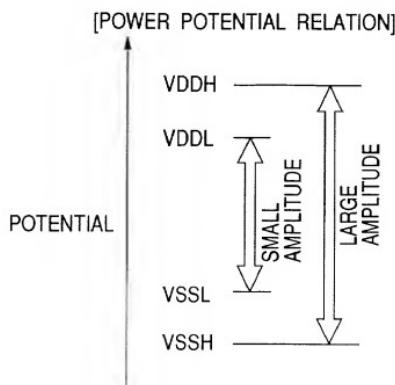
FIG. 23

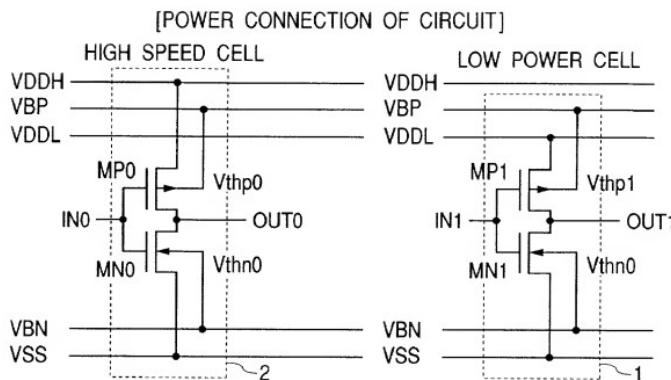
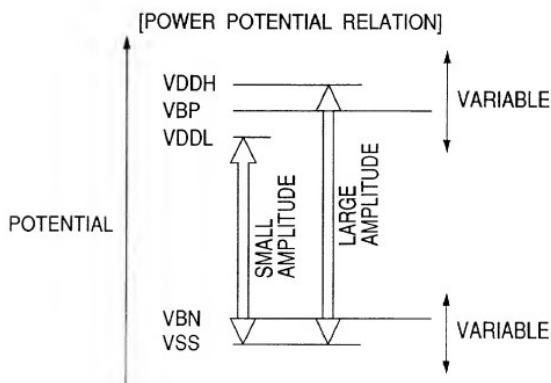


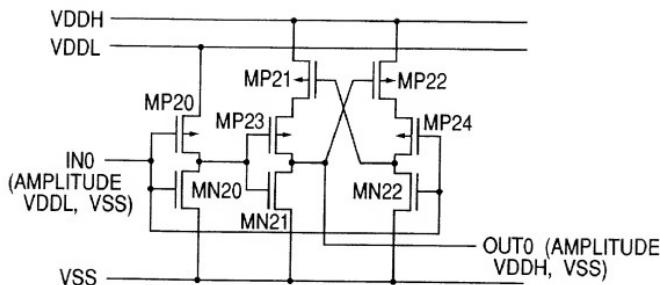
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FIG. 24



**FIG. 25****FIG. 26**

**FIG. 27****FIG. 28**

**FIG. 29****FIG. 30**